Abstract of the Disclosure

A level shift circuit includes first and second inverters and an inversion circuit. The first inverter has a first input terminal and a first output terminal for generating the output signal. The first inverter includes a first transistor having a first current driving capacity. The second inverter has a second input terminal connected to the first output terminal and a second output terminal connected to the first input terminal. The second inverter includes a second transistor having a second current driving capacity smaller than the first capacity. The inversion circuit has an output terminal connected to the first input terminal. The inversion circuit receives an input signal including a first input signal and a second input signal one of which is a one-shot pulse signal. The inversion circuit includes a third transistor having a third current driving capacity smaller than the first capacity and larger than the second capacity.